In the Abstract:

Please amend the Abstract of Disclosure as follows:

Disclosed is a method for manufacturing multi-level interconnections using a dual damascene process. The method includes: forming a first interconnection line in a second interlayer insulating layer and a first etching stop layer sequentially formed on a first interlayer insulating layer disposed on a semiconductor substrate; forming a ~~first~~ third interlayer insulating layer on the first interconnection line and second interlayer insulating layer; forming a ~~first~~ second etching stop layer on the ~~first~~ third interlayer insulating layer; forming a via hole exposing the first interconnection line by selectively etching the ~~first~~ second etching stop layer and the ~~first~~ third interlayer insulating layer; forming etching stop patterns around an inlet of the via hole by selectively etching the ~~first~~ second etching stop layer; forming a ~~second~~ fourth interlayer insulating layer on the etching stop ~~pattern~~ patterns and the ~~first~~ third interlayer insulating layer; forming a trench by selectively etching the ~~second~~ fourth interlayer insulating layer; and forming a conductive layer in the trench and in the via hole.